Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices

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ABSTRACT

This application note recommends power supply and ground noise-reduction techniques through the use of bypass capacitors and ferrite beads in TI's PLL-based clock distribution circuits (CDC) devices. This application note also includes a numeric example, calculating the value of bypass and filter capacitors for a particular frequency of interest.

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Bypass and Filter Capacitors

Practically all circuits use dc (direct current) supplies for their inputs. However, dc voltage may fluctuate producing ac ripple voltage and noise components. If the ripple voltage is too high, it renders the circuit nonfunctional. The main function of bypass capacitors is to dampen this ac ripple component or noise in such dc circuits. The first function of a bypass capacitor connected between VDD and GND is to allow the ac ripple component of VDD to pass through to ground. The second function is to help compensate for voltage droop caused by large I_{CC} transients when multiple outputs switch simultaneously. The exact value of a bypass capacitor is not as important as the frequency at which this ripple occurs. Use a minimum of three bypass capacitors, each targeting a slightly different frequency. As an example, use a large capacitor between 4.7 μF to 47 μF to target large voltage droops at relatively low frequency. Choose a smaller value (about 0.1 μF) for middle frequency range, and an even smaller value bypass capacitor (around 0.01 μF) to handle higher frequencies. It is more effective to use an array of three or more bypass capacitors with different capacitance values when filtering a wider noise bandwidth. The frequency response of any capacitor is determined by its parasitics, that is, its equivalent series resistance (ESR) and equivalent series inductance (ESL). These two parameters are most important when choosing a bypass capacitor. Use high-quality, surface-mount capacitors. Monolithic or ceramic type capacitors feature both low ESR, ESL, and consequently achieve excellent performance.

The distinction between a filter and a bypass capacitor depends on where it is being used. When used to eliminate low-frequency power-supply noise, it is referred to as a filter capacitor. An example is a 22-μF capacitor connected between VDD and GND. On the other hand, bypass capacitors are used at high frequency to provide a very low-impedance path for current surges between VDD and GND, as well as to guard power systems against induced fluctuations.

General Guidelines for Calculating the Value of a Bypass Capacitor [6]

1. First, assuming all gates are switching simultaneously in a system, find the maximum expected step change in power supply current ΔI.
2. Estimate the maximum amount of noise that a given system can tolerate from the system's noise budget.
3. Dividing the noise voltage by the current change gives the maximum common path impedances, $Z_{\max} = V_n / \Delta I$.
4. Next, compute the inductance (L_{PSW}) of power supply wiring. Use this and $Z_{\max}$ to find the frequency, $f_{PSW} = f_{(corner)} = f_{3dB} = Z_{\max} / (2\pi L_{PSW})$ below which the power supply wiring is fine (power supply noise<V_n).
5. Finally, calculate the capacitance (C_{bypass}) of the bypass capacitor: $C_{bypass} = 1/2\pi\ f_{PSW}\ Z_{\max}$

NOTE: If the operating frequency is $f_{(oper)} < f_{PSW}$, then it is not necessary to use a bypass capacitor. On the other hand, if it is $f_{(oper)} \geq f_{PSW}$, then it is necessary to use a bypass capacitor. Please refer to the example below.

Example

Let us assume that: (1) we have a board of 50 gates (output buffers) each switching a 15-pF load in 2.4 ns, (2) a power supply wiring inductance of L = 110 nH, (3) a power supply of V_{CC} = 3.3 V, and (4) a 120-mV noise margin ($V_n = 120mV$).

Then current is: $\Delta I = n\,C\,\frac{Vcc}{\Delta t} = \frac{(50)\,(15\times10^{-12})\,(3.3)}{2.4\times10^{-9}} = 1.03125\ A$

The maximum impedance, $Z_{\max} = \frac{V_n}{\Delta I} = \frac{120mV}{1.03125} = 0.116364\ \Omega$

Then, the frequency (f_{PSW}) above which the power supply wiring needs a bypass capacitor,

$$f_{PSW} = \frac{Z_{\max}}{2\times\pi\times L_{PSW}} = \frac{0.116364\,\Omega}{2\times\pi\times110\times10^{-9}} = 168.363\ KHz$$

Finally, the value of the bypass capacitor is calculated according to:

$$C_{bypass\,(\min)} = \frac{1}{2\times\pi\times f_{PSW}\times Z_{\max}} = \frac{1}{2\pi\times168.363\times10^{3}\times0.116364} = 8.1237\,\mu F$$

This capacitance value is not common, so we can use 8 μF or 10 μF. This calculation shows that the 8 μF is effective at a frequency above 168.363 kHz.

Assuming that our bypass capacitor has an ESL of 1 nH, we can calculate the upper frequency range at which this capacitor will work as intended.

$$f_{bypass} = \frac{Z_{\max}}{2\,\pi\times ESL} = \frac{0.116364}{(2\,\pi\times1\times10^{-9})} = 18.52\ MHz$$

Therefore, this 8-μF bypass capacitor is effective from 168 kHz to 18.5 MHz.

It is common practice to use an array of small parallel capacitors; this combination provides lower series inductance at high frequency than a single bigger capacitor.

The most common values bypass capacitors are: 47 μF, 22 μF, 4.7 μF, 0.1 μF, and 0.001 μF. The higher value capacitors (47 μF and 4.7 μF) work well at relatively low frequency (low-frequency bypass). The 0.1 μF targets the middle frequency range, while the 0.001 μF or smaller capacitors handle higher frequencies (high frequency bypass). Choosing two or three capacitors with different capacitance ranges will effectively filter a wider noise bandwidth.

Real capacitors are not ideal; they are exemplified by additional parasitics (non-ideal) in the form of inductive and resistive elements. The most important elements are ESL and ESR; they act as an inductor and resistor in series with a capacitor, respectively. They act to defeat the effectiveness of a bypass capacitor.

The complete impedance equation of a capacitor as a function of frequency, including ESR, is:

$X(f) = \sqrt{ESR^2 + (2\pi fL - \frac{1}{2\pi fC})^2}$; Where $L = lead\ induc\tan ce, H$ and C = capacitance, F

ESR is usually included in a manufacturer's data sheet. It can be measured using ESR meters that can measure low resistance (below 1 Ω). However, methods of measuring ESR without ESR meters are available at [4]: http://fribble.cie.rpi.edu/~repairfaq/sam/captest.htm

Table 1 lists some suggested capacitor values targeting various frequency bypasses using the following equation:

$$f_{PSW} = \frac{1}{2 \times \pi \times C_{bypass(\min)} \times Z_{\max}}$$

Table 1. Capacitance to Filter Corresponding Noise Frequency

$C_{bypass\ (min)}$ [µF]	Frequency f_{PSW} @ Z_{max} = 0.1 Ω	Frequency f_{PSW} @ Z_{max} = 0.2 Ω
47	33.8 kHz	16.93 kHz
22	72 kHz	36 kHz
10	159 kHz	79.6 kHz
4.7	339 kHz	169.5 kHz
0.5	3.2 MHz	1.6 MHz
0.22	7.2 MHz	3.6 MHz
0.1	16 MHz	8 MHz
0.05	32 MHz	16 MHz
0.02	80 MHz	40 MHz
0.016	100 MHz	50 MHz
0.01	160 MHz	80 MHz
0.008	200 MHz	100 MHz
0.005	318 MHz	159 MHz
0.004	398 MHz	199 MHz
0.001	1.592 GHz	796 MHz

Decoupling

All decoupling capacitors should be placed as close as possible to each power supply pin. Typically, 0.1-µF capacitors should be connected between each VDD pin and ground.

Use a size 0603, high quality, low-inductance, low-ESR, surface-mount capacitors. Furthermore, capacitors should be of either a ceramic or monolithic type for optimal performance. The value of decoupling capacitor is strongly dependent on the frequency of the clock driver. It is also dependent on noise generated at higher frequency harmonics. The rule of thumb is the higher the frequency, the lower the capacitance.

Ferrite Beads

Clock drivers typically produce switching noise. There is a need to isolate this noise component and prevent it from spreading into the PCB board. Inserting a ferrite bead between the clock driver's power supply and the main PCB power plane is an excellent method to effectively eliminate this problem. The ferrite bead does not enhance nor degrade the performance of the driver; it is only used to provide noise isolation. Ferrite beads are composed of a ferromagnetic material and are not susceptible to external radiated magnetic fields. They cannot be easily de-tuned. Only when the temperature rises above the Curie point will the ferrite lose its magnetic properties, rendering it useless. The Curie point is material dependent, ranging from 120°C to 500°C.

When selecting a ferrite, always know the frequency of the unwanted noise. In addition, the impedance of the ferrite is a function of frequency, size, material, and number of turns. The dc impedance of the ferrite should be close to zero. While at the clock frequency, the impedance should be greater than 50 Ω under loaded conditions. This relatively large impedance is necessary to prevent noise cased by clock harmonics from spreading to the PCB board. In addition, ferrite beads should be capable of providing the rated dc current to the VCC plane.

Filtering and Noise Reduction Circuits

Figures 1 and 2 below depict two recommended filter circuits for TI's CDC clock drivers. These circuits can be used with any PLL-based clock generator in which the PLL has both digital (VDD) and analog (AVDD) power supplies. Figure 1 is recommended where there is no board space constraint, while Figure 2 is the choice where there is limited board space.

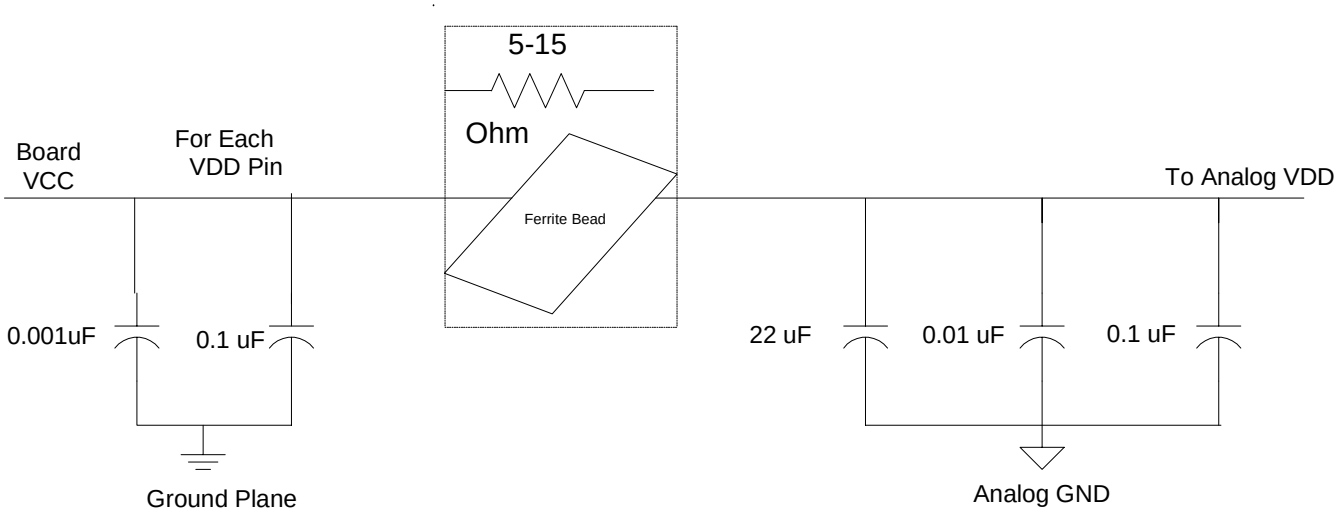

Figure 1. Filter Circuit 1

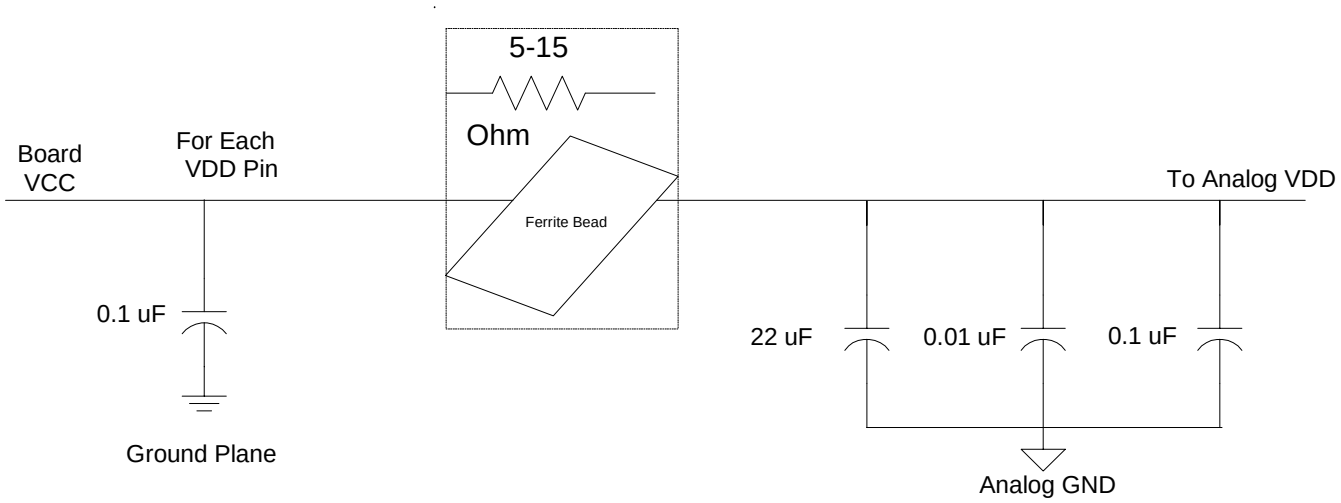

Figure 2. Filter Circuit 2

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6. Johnson, H.W., and Gram, M. *High-Speed Digital Design*. Prentice Hall, 1993.

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